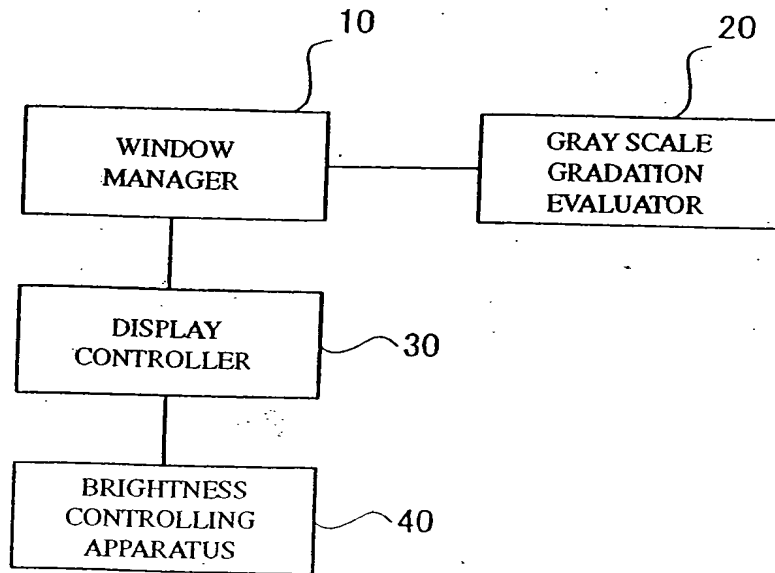


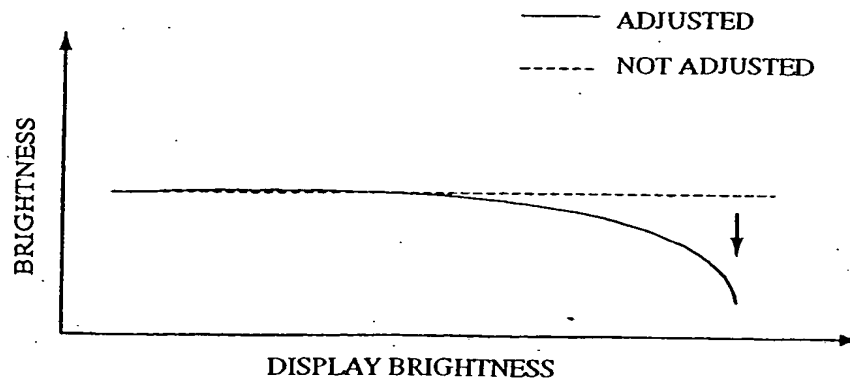
[Figure 1]

(1/9)

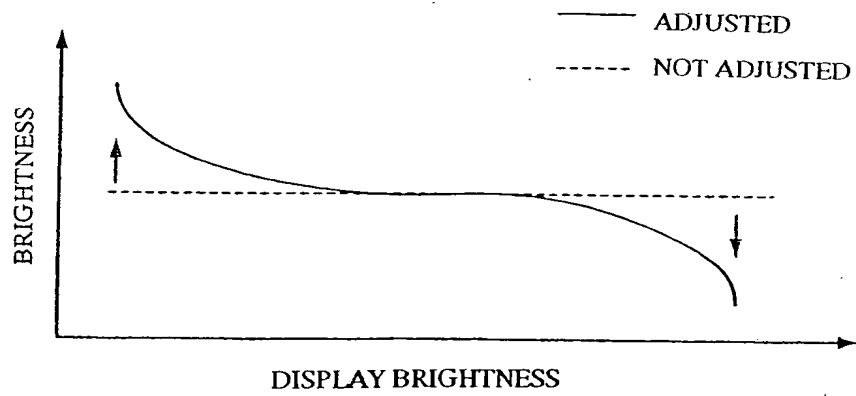


[Figure 2]

(2/9)

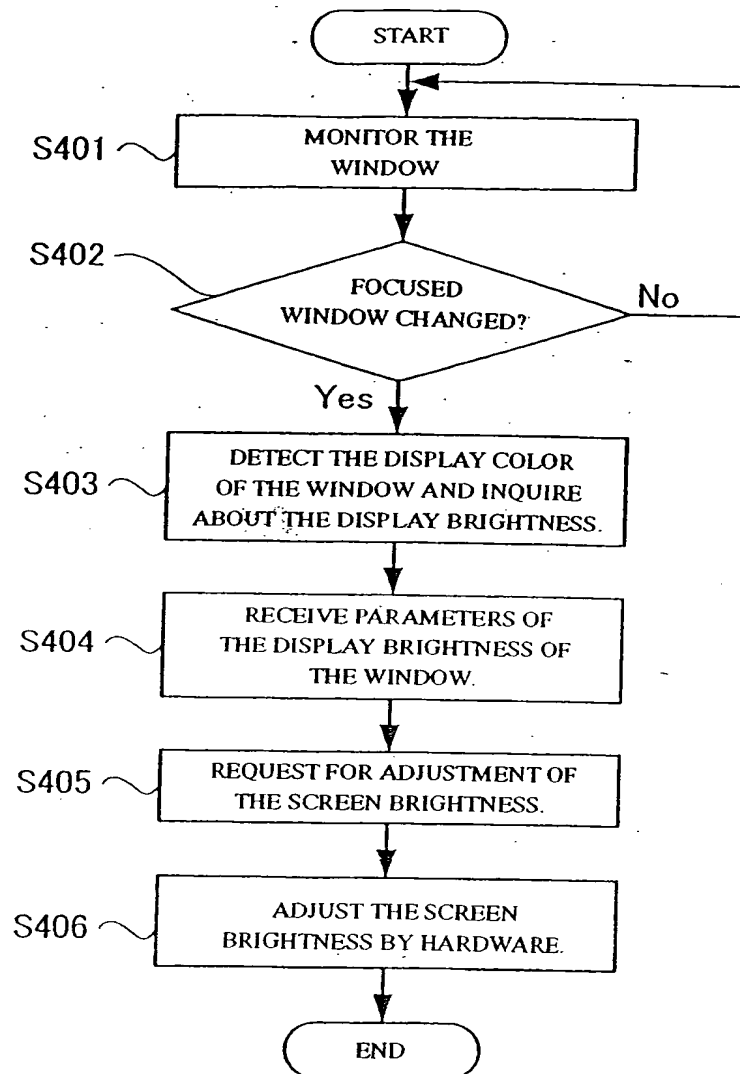


[Figure 3]



[Figure 4]

(3/9)



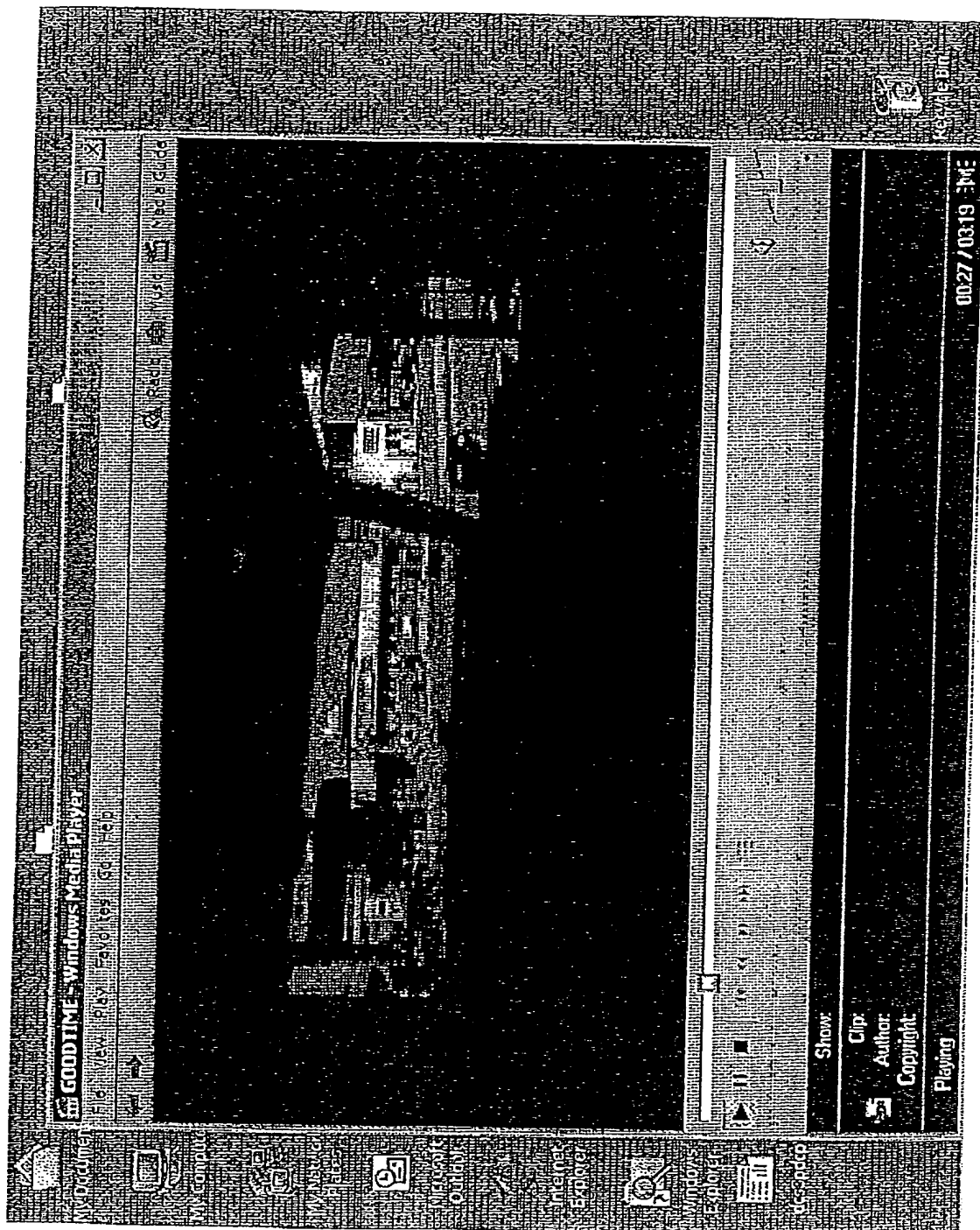
**intel**

**82371AB PCI-to-ISA / IDE  
XCELERATOR (PIIX4)**

- Supported Kits for both Pentium™ and Pentium™ Microprocessors
  - 82430TX ISA Kit
  - 82440LX ISA/DP Kit
- Multifunction PCI to ISA Bridge
  - Supports PCI at 30 MHz and 33 MHz
  - Supports PCI Rev 2.1 Specification
  - Supports Full ISA or Extended I/O (EO) Bus
  - Supports Full Positive Decode or Subtractive Decode of PCI
  - Supports ISA and EIO at 1/4 of PCI Frequency
- Supports both Mobile and Desktop Deep Green Environments
  - 3.3V Operation with 5V Tolerant Buffers
  - Ultra-low Power for Mobile Environments Support
  - Power-On Suspend, Suspend to RAM, Suspend to Disk, and Soft-Off System States
  - All Registers Readable and Restorable for Proper Resume from 0.V Suspend
- Power Management Logic
  - Global and Local Device Management
  - Suspend and Resume Logic
  - Supports Thermal Alarm
  - Support for External Microcontroller
  - Full Support for Advanced Configuration and Power Interface (ACPI) Revision 1.0 Specification and OS Directed Power
- Integrated 16 x 32-bit Buffer for IDE PCI Burst Transfers
  - Supports Glue-less "Swap-Bay" Option with Full Electrical Isolation
- Enhanced DMA Controller
  - Two 82C37 DMA Controllers
  - Supports PCI DMA with 3 PQIRCI Channels and Distributed DMA Protocol (Simultaneous)
  - Fast Type-F DMA for Reduced PCI Bus Usage
- Interrupt Controller Based on Two 82C59
  - 15 Interrupt Support
  - Independently Programmable for Edge-Level Sensitivity
  - Supports Optional I/O APIC
  - Serial Interrupt Input
- Timers Based on 82C54
  - System Timer, Refresh Request, Speaker Tone Output
- USB
  - Two USB 1.0 Ports for Serial Transfers at 12 or 1.5 Mbit/sec.
  - Supports Legacy Keyboard and Mouse Software with USB-based Keyboard and Mouse
  - Supports UHCI Design Guide
- SMBus
  - Host Interface Allows CPU to Communicate Via SMBus
  - Slave Interface Allows External SMBus Master to Control Resume Events
- Real-Time Clock

[Figure 6]

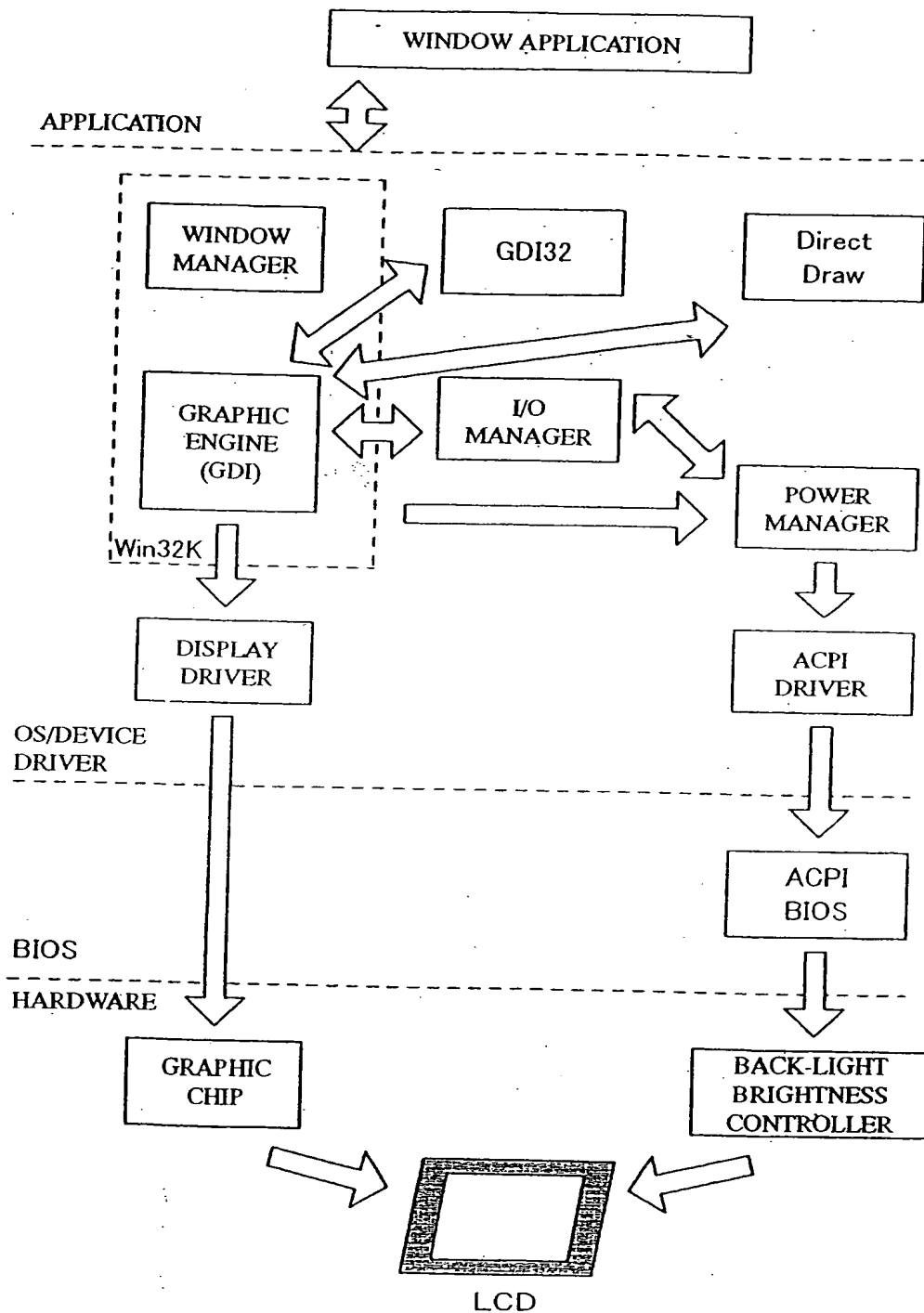
(5/9)



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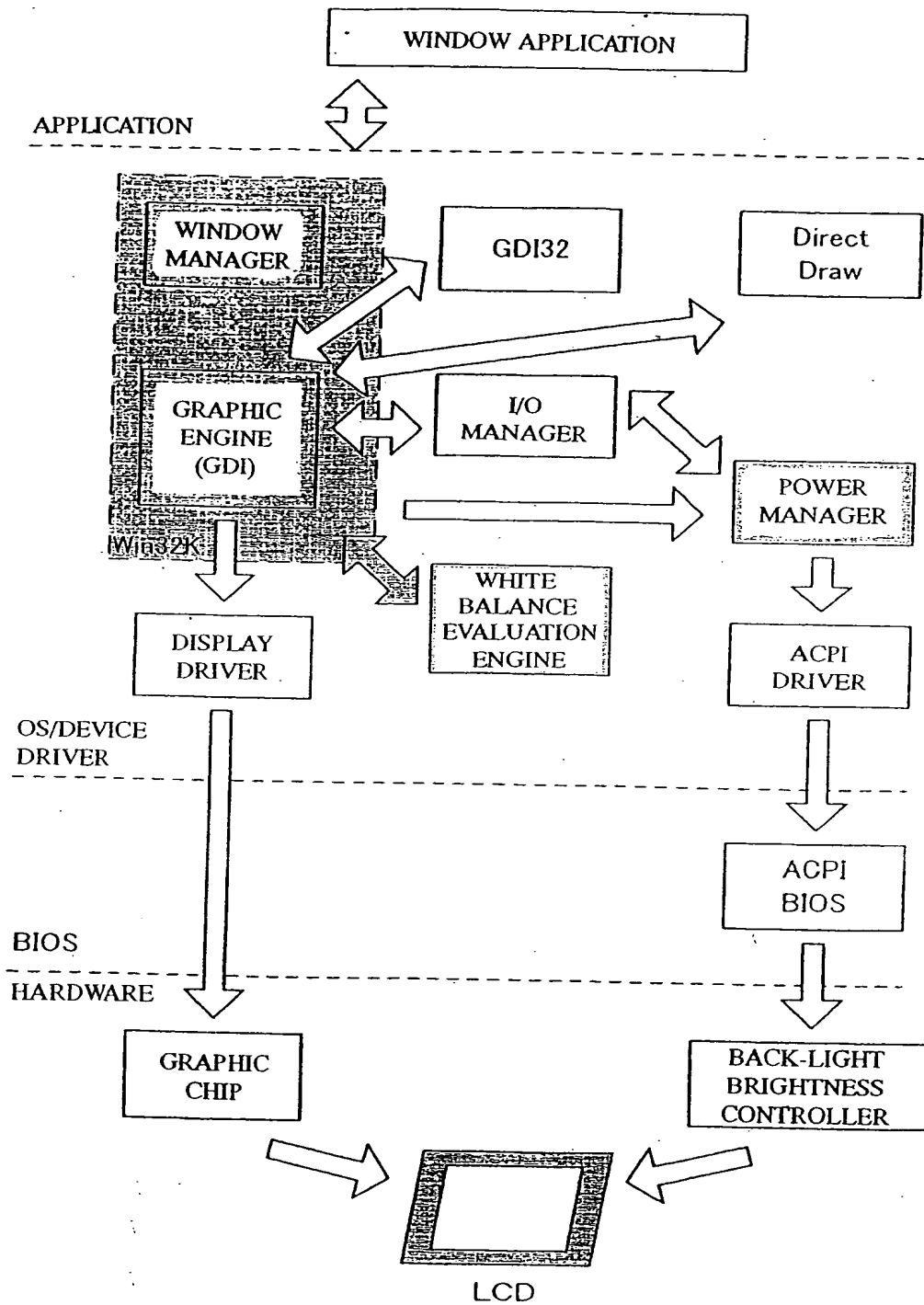
[Figure 7]

(6/9)



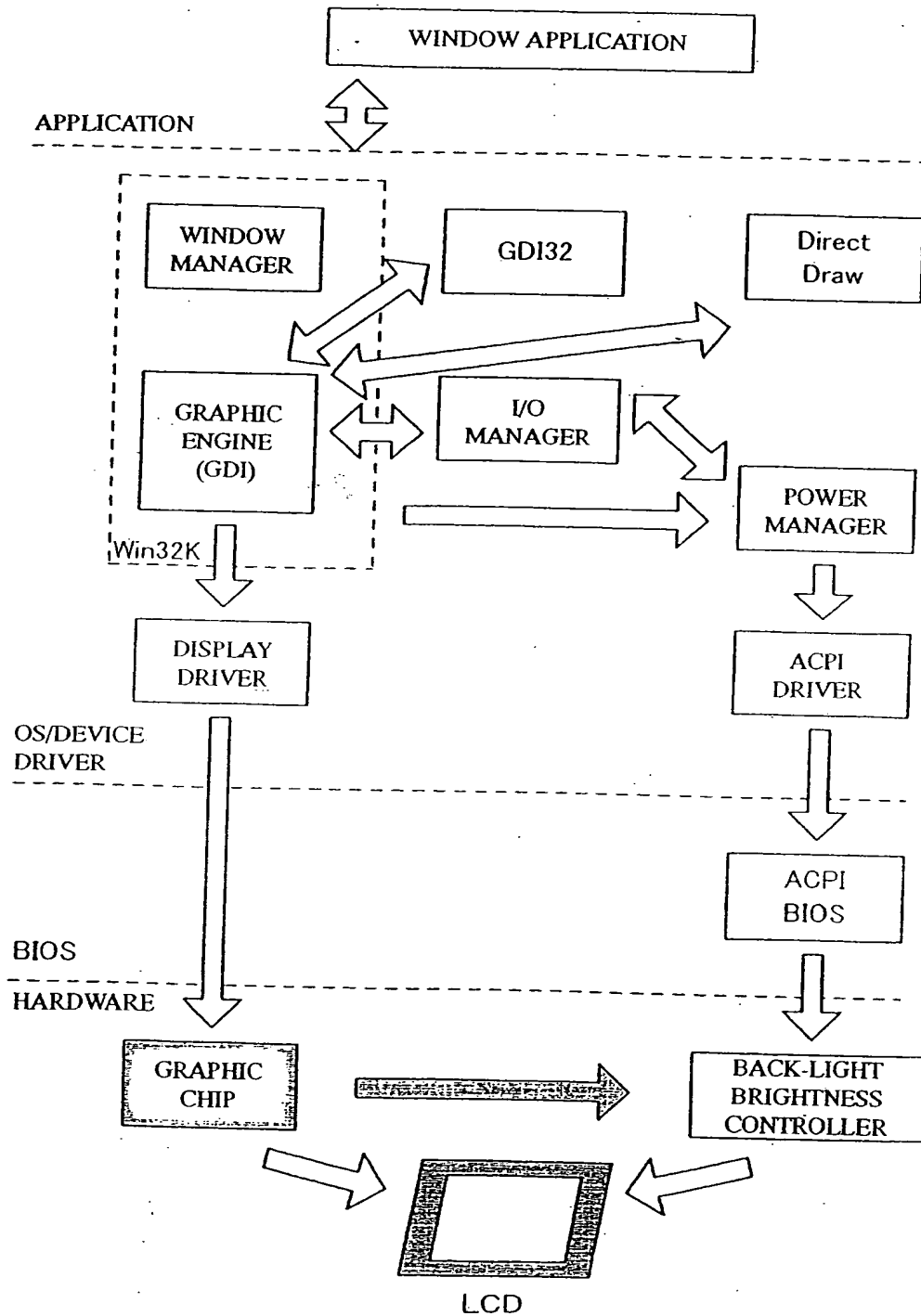
[Figure 8]

(7/9)



[Figure 9]

(8/9)





[Figure 10]

(9/9)

